The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1-8. (Cancelled).

9. (Currently Amended) A charge pump circuit comprising:

a charge pumping unit having first and second input terminals, a bias terminal, and an output terminal, said charge pumping unit charging and discharging a capacitor connected to said output terminal, and setting up the current flowing to said output terminal in response to bias voltage applied to said bias terminal of said charge pumping unit;

a current mirror unit having a bias terminal and an output terminal, said current mirror receiving a current flowing to said output terminal of said charge pumping unit, and controlling a voltage of said output terminal in response to bias voltage applied to said bias terminal of said current mirror unit;

a control unit having a first input terminal connected to said output terminal of said charge pumping unit, a second input terminal connected to said output terminal of said circuit mirror unit, and an output terminal, said control unit controlling a control current flowing to said output terminal of said control unit in response to a difference of voltage between said first and said second input terminals of said control unit, ~~said control unit having a comparator controlling a voltage of said output terminal of said control unit by a difference of the voltage applied to said first and second input terminals~~; and

a biasing unit having a control terminal connected to said output terminal of said control unit, an output terminal connected to said bias terminal of said charge pumping

unit[[,]] and said bias terminal of said current mirror unit, and controlling a voltage of said output terminal of said biasing unit in response to said control current flowing to said control terminal of said biasing unit.

10. (Currently Amended) The A charge pump circuit comprising:

a charge pumping unit having first and second input terminals, a bias terminal, and an output terminal, said charge pumping unit charging and discharging a capacitor connected to said output terminal, and setting up the current flowing to said output terminal in response to bias voltage applied to said bias terminal of said charge pumping unit, said charge pumping unit including first and second PMOS transistors and first and second NMOS transistors,

gates of said first PMOS and NMOS transistors respectively forming said first and second input terminals of said charge pumping unit,

drains of said first PMOS and NMOS transistors being respectively connected to sources of said second PMOS and NMOS transistors, sources of said first PMOS and NMOS transistors being respectively connected to a power source and a ground, and

a gate of said second PMOS transistor forming said bias terminal of said charge pumping unit and being connected to said biasing unit and forming said output terminal of said charge pumping unit, a constant N type bias voltage being applied to a gate of said second NMOS transistor;

a current mirror unit having a bias terminal and an output terminal, said current mirror receiving a current flowing to said output terminal of said charge pumping unit, and controlling a voltage of said output terminal in response to bias voltage applied to said bias terminal of said current mirror unit;

a control unit having a first input terminal connected to said output terminal of said charge pumping unit, a second input terminal connected to said output terminal of said circuit mirror unit, and an output terminal, said control unit controlling a control current flowing to said output terminal of said control unit in response to a difference of voltage between said first and said second input terminals of said control unit; and

a biasing unit having a control terminal connected to said output terminal of said control unit, an output terminal connected to said bias terminal of said charge pumping unit[[,]] and <u>said bias terminal of</u> said current mirror unit, and controlling a voltage of said output terminal of said biasing unit in response to said control current flowing to said control terminal of said biasing unit.

11. (Currently Amended) A charge pump circuit comprising:

a charge pumping unit having first and second input terminals, a bias terminal, and an output terminal, said charge pumping unit charging and discharging a capacitor connected to said output terminal, and setting up the current flowing to said output terminal in response to bias voltage applied to said bias terminal of said charge pumping unit;

a current mirror unit having a bias terminal and an output terminal, said current mirror receiving a current flowing to said output terminal of said charge pumping unit, and controlling a voltage of said output terminal in response to bias voltage applied to said bias terminal of said current mirror unit, said current mirror unit including first and second PMOS transistors and first and second NMOS transistors,

gates of said first PMOS and NMOS transistors being respectively connected to ground and power sources, drains of said first PMOS and NMOS transistors being respectively connected to sources of said second PMOS and NMOS transistors,

sources of said first PMOS and NMOS transistors being respectively connected to a power source and a ground, and

said gate of said second PMOS transistor forming said bias terminal of said current mirror unit, and said drain of said second PMOS transistor being connected to said drain of said second NMOS transistor and forming said output terminal of said current mirror unit, said N type bias voltage being applied to said gate of said second NMOS transistor;

a control unit having a first input terminal connected to said output terminal of said charge pumping unit, a second input terminal connected to said output terminal of said circuit mirror unit, and an output terminal, said control unit controlling a control current flowing to said output terminal of said control unit in response to a difference of voltage between said first and said second input terminals of said control unit; and

a biasing unit having a control terminal connected to said output terminal of said control unit, an output terminal connected to said bias terminal of said charge pumping unit[[,]] and <u>said bias terminal of</u> said current mirror unit, and controlling a voltage of said output terminal of said biasing unit in response to said control current flowing to said control terminal of said biasing unit.

12. (Currently Amended) The charge pump circuit according to claim 9, wherein said control unit has ±input terminals that form said first and second input terminals of said control unit, and <u>includes a</u> ~~said~~ comparator ~~controls~~ <u>to control</u> a voltage of said output terminal by a difference of the voltage applied to said ±input terminals and a PMOS transistor, and

a source of said PMOS transistor is connected to power source, and a gate of said PMOS transistor is connected to said output terminal of said comparator, and a drain of said PMOS transistor forms said output terminal of said control unit.

13. (Currently Amended) A charge pump circuit comprising:

a charge pumping unit having first and second input terminals, a bias terminal, and an output terminal, said charge pumping unit charging and discharging a capacitor connected to said output terminal, and setting up the current flowing to said output terminal in response to bias voltage applied to said bias terminal of said charge pumping unit;

a current mirror unit having a bias terminal and an output terminal, said current mirror receiving a current flowing to said output terminal of said charge pumping unit, and controlling a voltage of said output terminal in response to bias voltage applied to said bias terminal of said current mirror unit;

a control unit having a first input terminal connected to said output terminal of said charge pumping unit, a second input terminal connected to said output terminal of said circuit mirror unit, and an output terminal, said control unit controlling a control current flowing to said output terminal of said control unit in response to a difference of voltage between said first and said second input terminals of said control unit; and

a biasing unit having a control terminal connected to said output terminal of said control unit, an output terminal connected to said bias terminal of said charge pumping unit[[,]] and <u>said bias terminal of</u> said current mirror unit, and controlling a voltage of said output terminal of said biasing unit in response to said control current flowing to said control terminal of said biasing unit, said biasing unit including first and second PMOS transistors and first and second NMOS transistors, and gates of said first PMOS and NMOS transistors

being respectively connected to ground and power sources, drains of said first PMOS and NMOS transistors being respectively connected to sources of said second PMOS and NMOS transistors, and sources of said first PMOS and NMOS transistors being respectively connected to a power source and a ground, and

said gate of said second PMOS transistor forming said output terminal of said biasing unit, said drain of said second PMOS transistor being connected to said source of said second NMOS transistor and being said control terminal of said biasing unit, said gate and drain of said second PMOS transistor being connected to each other, and said N type bias voltage being applied to said gate of said second NMOS transistor.

14. (Previously Presented) The charge pump circuit of claim 9, wherein said charge pumping unit includes first and second PMOS transistors and first and second NMOS transistors, and gates of said first PMOS and NMOS transistors respectively form said first and second input terminals of said charge pumping unit, drains of said first PMOS and NMOS transistors are respectively connected to a power source and a ground, and

a gate of said second NMOS transistor forms said bias terminal of said charge pumping unit, a drain of said second NMOS transistor is connected to said biasing unit and forms said output terminal of said charge pumping unit, and a constant P type bias voltage is applied to said gate of said second PMOS transistor.

15. (Previously Presented) The charge pump circuit according to claim 9, wherein said current mirror unit includes first and second PMOS transistors and first and second NMOS transistors, gates of said first PMOS and NMOS transistors are respectively connected to a ground and a power source, and drains of said first PMOS and NMOS

transistors are respectively connected to sources of said second PMOS and NMOS transistors, and sources of said first PMOS and NMOS transistors are respectively connected to a power source and a ground, and

said gate of said second NMOS transistor forms said bias terminal of said current mirror unit, and said drain of said second NMOS transistor is connected to said drain of said second PMOS transistor and forms said output terminal of said current mirror unit, and said P type bias voltage is applied to said gate of said second PMOS transistor.

16. (Previously Presented) The charge pump circuit according to claim 9, wherein said control unit has ±input terminals that form said first and second input terminals of said control unit, said control unit includes a comparator that controls voltage of said output terminal by a difference of the voltage applied to said ±input terminals and an NMOS transistor, and

a source of said NMOS transistor is grounded, a gate of said NMOS transistor is connected to said output terminal of said comparator, and a drain of said NMOS transistor forms said output terminal of said control unit.

17. (Previously Presented) The charge pump circuit according to claim 9, wherein said biasing unit includes first and second PMOS transistors and first and second NMOS transistors, gates of said first PMOS and NMOS transistors are respectively connected to a ground and a power source, drains of said first PMOS and NMOS transistors are respectively connected to sources of said second PMOS and NMOS transistors, and sources of said first PMOS and NMOS transistors are respectively connected to a power source and a ground, and

said gate of said second NMOS transistor forms said output terminal of said biasing unit, said source of said second NMOS transistor is connected to said drain of said second PMOS transistor and forms said control terminal of said biasing unit, and said gate and drain of said second NMOS transistor are connected to each other, and said P type bias voltage is applied to said gate of said second PMOS transistor.